

RJJ0601JPE

Silicon P Channel MOS FET
High Speed Power Switching

REJ03G1603-0100

Rev.1.00

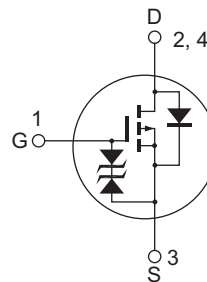
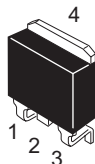
Nov 21, 2007

Features

- Low on-resistance
 $R_{DS(on)} = 8.2 \text{ m}\Omega$ typ.
- Capable of 4.5 V gate drive
- High speed switching

Outline

RENESAS Package code: PRSS0004AE-B
(Package name: LDKPAK(S)-(1))



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	-60	V
Gate to source voltage	V_{GSS}	± 20	V
Drain current	I_D	-90	A
Drain peak current	I_D (pulse) ^{Note1}	-360	A
Body-drain diode reverse drain current	I_{DR}	-90	A
Avalanche current	I_{AP} ^{Note3}	-40	A
Avalanche energy	E_{AR} ^{Note3}	137	mJ
Channel dissipation	P_{ch} ^{Note2}	90	W
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

Notes: 1. $PW \leq 10 \mu\text{s}$, duty cycle $\leq 1\%$

2. Value at $T_c = 25^\circ\text{C}$

3. Value at $T_{ch} = 25^\circ\text{C}$, $R_g \geq 50 \Omega$

Thermal Impedance Characteristics

- Channel to case thermal impedance θ_{ch-c} : 1.39°C/W

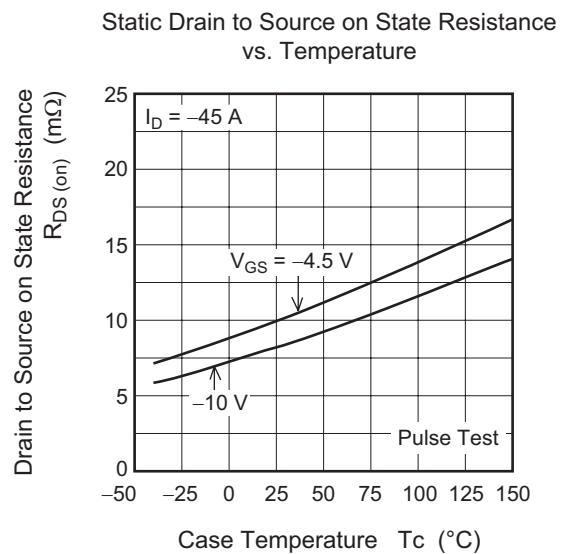
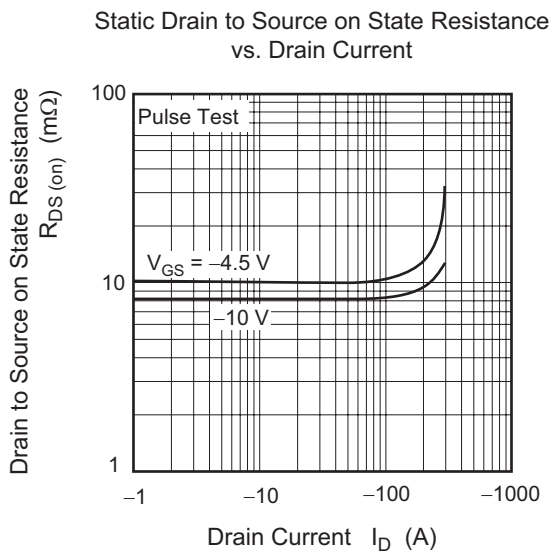
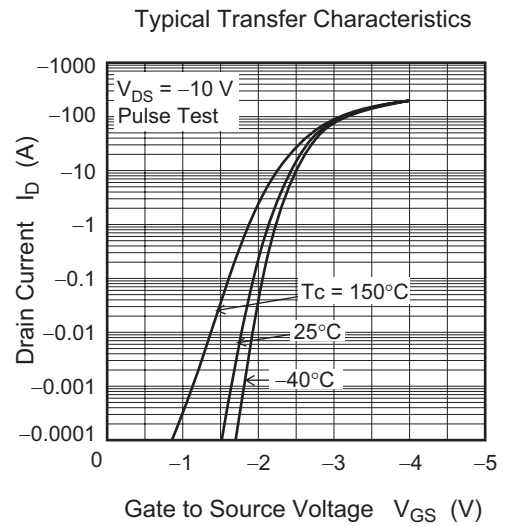
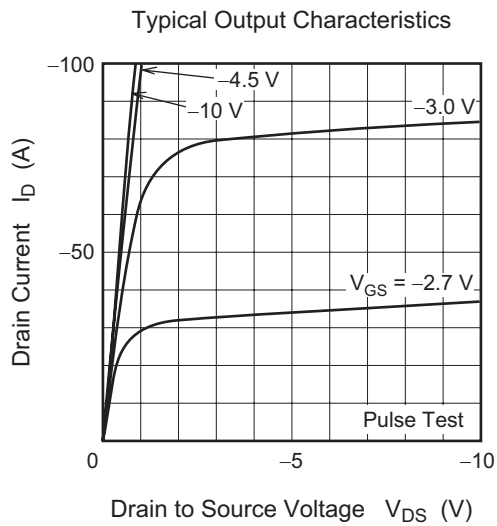
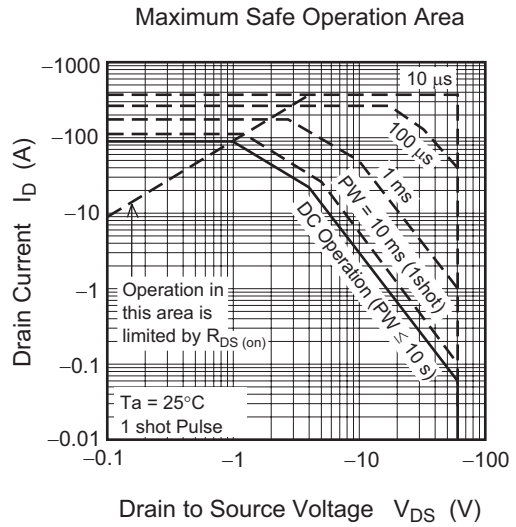
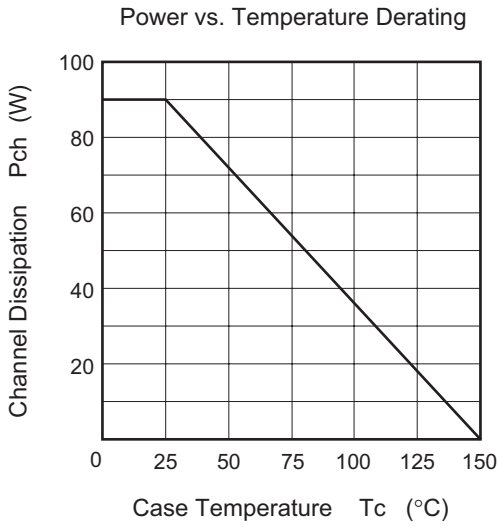
Electrical Characteristics

(Ta = 25°C)

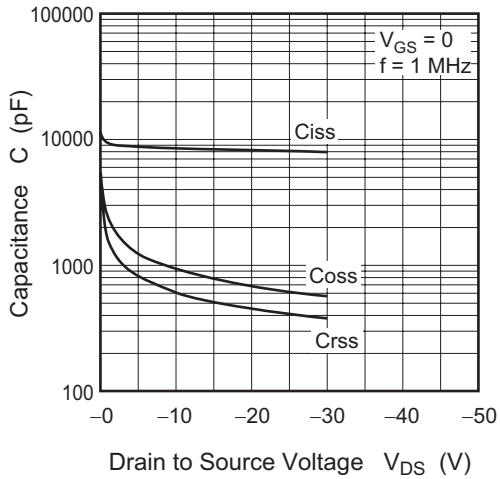
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-10	μA	$V_{DS} = -60 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	60	100	—	S	$I_D = -45 \text{ A}$, $V_{DS} = -10 \text{ V}$ ^{Note4}
Static drain to source on state resistance	$R_{DS(on)}$	—	8.2	11	$\text{m}\Omega$	$I_D = -45 \text{ A}$, $V_{GS} = -10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	10	15	$\text{m}\Omega$	$I_D = -45 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	8800	—	pF	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	950	—	pF	
Reverse transfer capacitance	C_{rss}	—	600	—	pF	
Total gate charge	Q_g	—	150	—	nC	$V_{DD} = -25 \text{ V}$, $V_{GS} = -10 \text{ V}$, $I_D = -90 \text{ A}$
Gate to source charge	Q_{gs}	—	25	—	nC	
Gate to drain charge	Q_{gd}	—	23	—	nC	
Turn-on delay time	$t_{d(on)}$	—	25	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -45 \text{ A}$, $V_{DD} = -30 \text{ V}$ $R_G = 4.7 \text{ }\Omega$
Rise time	t_r	—	30	—	ns	
Turn-off delay time	$t_{d(off)}$	—	290	—	ns	
Fall time	t_f	—	135	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.96	—	V	$I_F = -90 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	45	—	ns	$I_F = -90 \text{ A}$, $V_{GS} = 0$, $di_F/dt = 100 \text{ A}/\mu\text{s}$

Note: 4. Pulse test

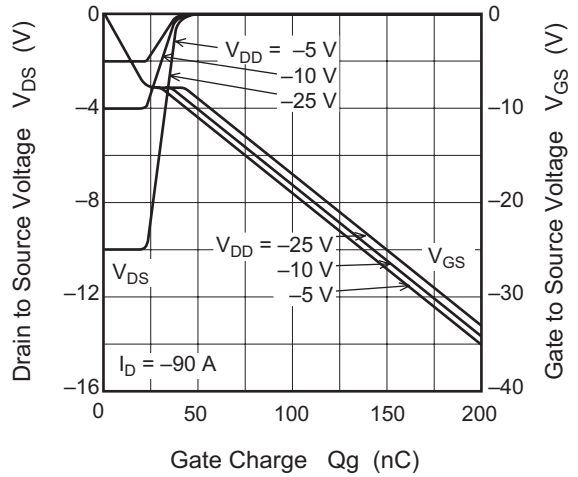
Main Characteristics



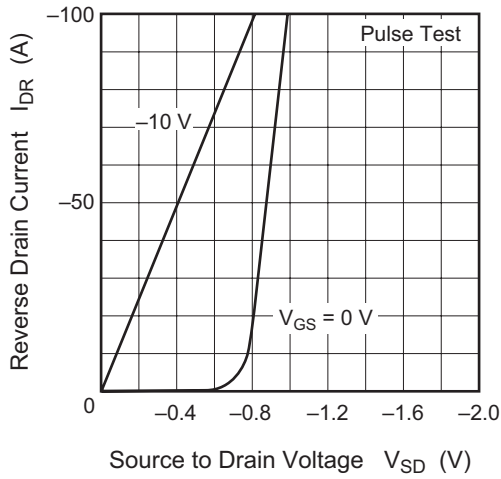
Typical Capacitance vs. Drain to Source Voltage



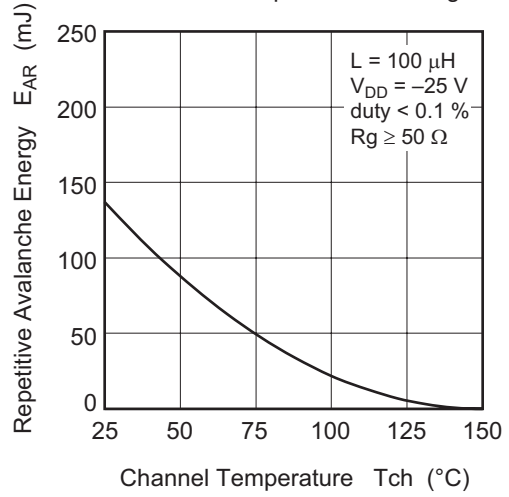
Dynamic Input Characteristics



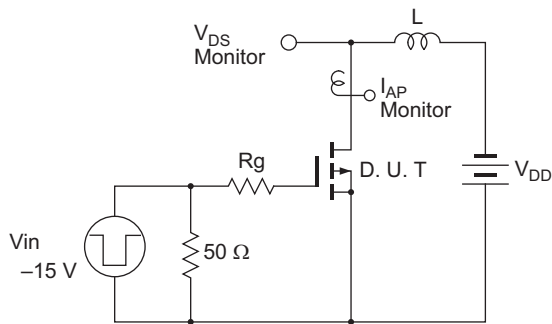
Reverse Drain Current vs. Source to Drain Voltage



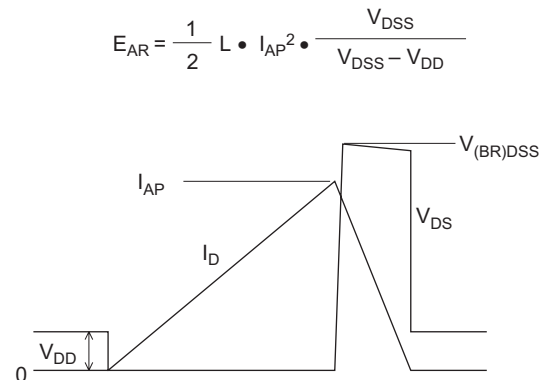
Maximum Avalanche Energy vs. Channel Temperature Derating

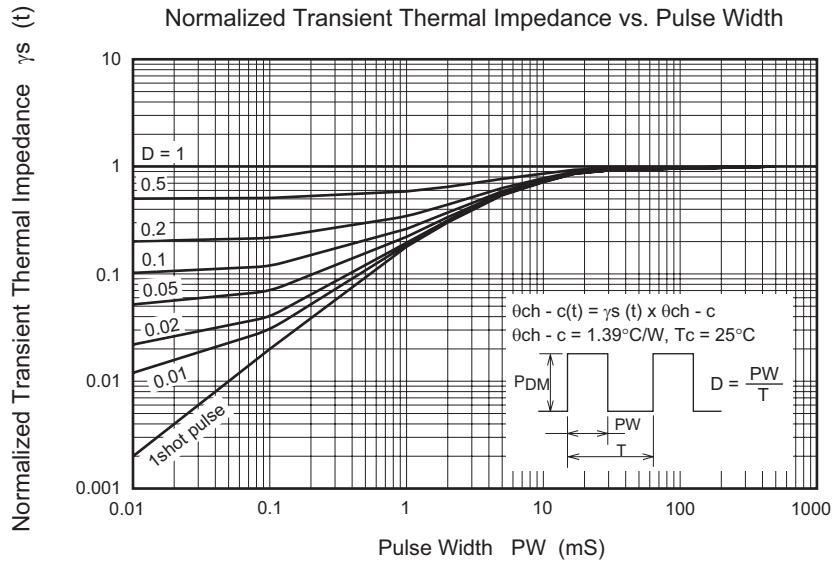


Avalanche Test Circuit

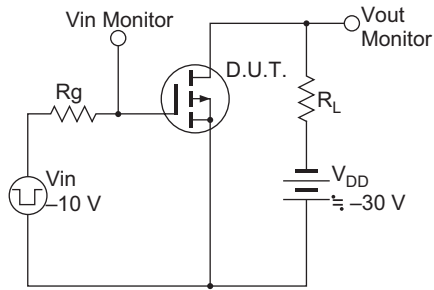


Avalanche Waveform

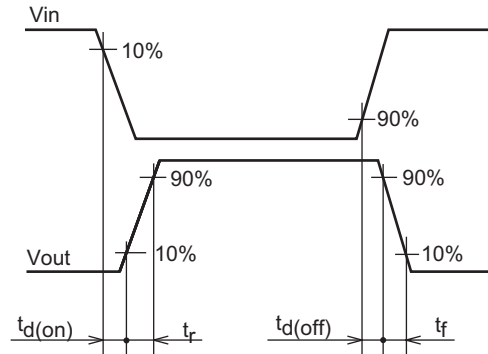




Switching Time Test Circuit

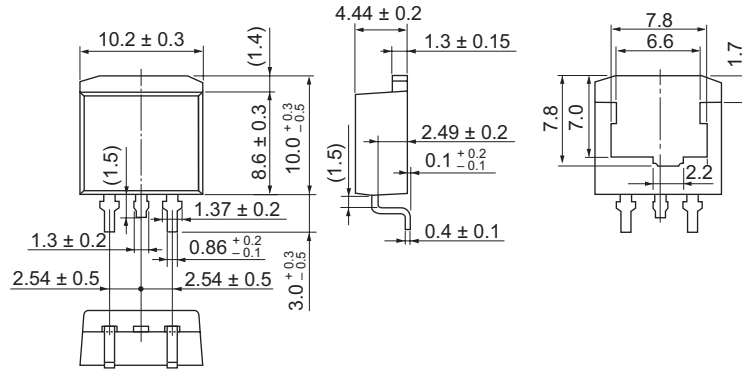


Switching Time Waveform



Package Dimensions

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]	Unit: mm
LDBPAK(S)-(1)	SC-83	PRSS0004AE-B	LDBPAK(S)-(1)/LDBPAK(S)-(1)V	1.30g	



Ordering Information

Part No.	Quantity	Shipping Container
RJJ0601JPE-00-Q3	1000 pcs	Taping (Dextrorse)
RJJ0601JPE-00-J3	1000 pcs	Taping (Sinistrorse)

Notes:

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